REMARKS

Preliminary Amendment Assumed Entered

A Preliminary Amendment directed to the present application was filed on March 8, 2001, along with a Information Disclosure Statement (IDS). The Office Action mailed December 1, 2003, indicates that the Action is "responsive to communication(s) filed on 06 October 2000," the filing date of the present application. However, Applicants have properly received an initialed copy of the Form 1449 filed with the IDS. **Therefore, Applicants assume that the Examiner has also received the Preliminary Amendment filed concurrently with the IDS, and that this Preliminary Amendment has been entered.** If this assumption is incorrect, Applicants respectfully request that the Examiner contact Applicants agent, Lois D. Cartier, at 720-652-3733.

Objections to the Abstract and Disclosure

The abstract has been objected to for exceeding 150 words. Applicants have amended the abstract to include less than 150 words.

The disclosure has been objected to because of certain informalities. Applicants have amended the disclosure to replace application serial numbers with patent numbers as suggested by the Examiner, thereby remedying these informalities.

No new matter is added.

Amendments to the Drawings

Applicants are enclosing proposed amendments to Figures 2A-2C in the same package as the present response. These amendments label Figures 2A-2C as prior art, as suggested by the Examiner.

Claims Rejections Under 35 USC 112

Claim 10 has been rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The Examiner claims "The specification does not support the claimed recitation of having adjustment of +2 prior to starting the pattern, where the pattern having the sequence of '+1, +2, 0, +2, -1, +2, -2, +2 and +2'".

Applicants respectfully traverse this rejection. Support for Claim 10 is found in the specification as originally filed at page 47, line 30 to page 48, line 7. Thus, Claim 10 meets the requirements of 35 U.S.C. 112, first paragraph.

Claims Rejections Under 35 USC 102(e)

Claims 1, 2 and 6 have been rejected under 35 U.S.C. 102(e) as being anticipated by Jeong (U.S. Patent No. 5,712,884).

Claim 1 has been amended to recite "enabling a first set of delay trim units …, thereby causing the generated clock signal to exhibit a first clock period during a first set of clock cycles; enabling a second set of delay trim units …, thereby causing the generated clock signal to exhibit a second clock period during a second set of clock cycles, wherein the second clock period is less than the first clock period; and enabling a third set of delay trim units …, thereby causing the generated clock signal to exhibit a third clock period during a third set of clock cycles, wherein the third clock period is greater than the first clock period, and wherein the first second and third sets of clock cycles are exhibited in a repeating regular pattern." Support for this amendment exists in the specification as originally filed at page 48, line 24 to page 49, line 2, and in Figs. 19A-19B. No new matter is added.

The Examiner indicates that Jeong teaches "the clock period is different for each clock period as shown in Fig. 6, which is identical to this application's Fig. 4." This statement is incorrect for the reasons set forth below.

Contrary to the Examiner's assertions, Jeong fails to teach or suggest that the clock signals CK0-CK9 illustrated in Fig. 6 have different clock periods. Jeong specifically indicates that the delay locked loop 12 includes "9 delay cells 22 for producing clocks CK1-CK9". "Each delay cell outputs a clock which delays an inputted clock by 2Π/10 radian (that is, 36°)." (Jeong, Col. 3, lines 21-28.) Jeong further states "Since each delay cell 22 … has the identical delay time, the clocks CK1-CK10 outputted from the secondary DLL 12 represents the clocks which delay the clock CK0 outputted from the first DLL 10 by 36° in order". (Jeong, Col. 3, lines 43-47)

The above-described relationship is shown in Fig. 6 of Jeong, which illustrates clock signals CK0-CK9. Note that clock signals CK0-CK9 appear to have the same clock period, even though the phases of these clock signals are successively offset by 36°. Because Jeong fails to teach or suggest clock signals having different clock periods, Jeong also fails to teach a "second clock period is less than" … a "first clock period", and, a "third clock period is greater than" … a "first clock period" as recited by Claim 1. In addition, Jeong fails to teach or suggest "the first, second and third sets of clock cycles are exhibited in a repeating regular pattern" as recited by Claim 1.

For these reasons, Claim 1 is not anticipated by Jeong. Claims 2 and 6, which depend from Claim 1, are not anticipated by Jeong for at least the same reasons as Claim 1.

Claims 1, 2, 5, 7-9, 17 and 18 have been rejected under 35 U.S.C. 102(e) as being anticipated by Matsuzaki et al. (U.S. Patent No. 6,194,930). Claim 5 has been canceled, thereby obviating the rejection of this claim.

Matsuzaki et al. teach a delay locked loop circuit, which delays a first clock, and generates a control clock having a predetermined phase relation with this first clock. (Matsuzaki et al., Col. 2, lines 30-33.) During power on, or standby mode recovery, a binary phase adjustment is performed to quickly

adjust the phase relation toward a lock-on state. (Matsuzaki et al., Col. 11, line 35 to Col. 12, line 55.) After this binary phase adjustment is performed, a single shift system is used to achieve and maintain a lock-on state. (Matsuzaki et al., Col. 12, line 57 to Col. 13, line 4.) This enables "lock-on time to be greatly shortened". (Matsuzaki et al., Col. 13, lines 5-20.)

While Matsuzaki et al. teaches binary and single step adjustment of clock phases, Matsuzaki et al. fails to teach or suggest "first, second and third sets of clock cycles are exhibited in a repeating regular pattern" as recited by Claim 1.

For these reasons, Claim 1 is not anticipated by Matsuzaki et al. Claim 2, which depends from Claim 1, is not anticipated by Matsuzaki et al. for at least the same reasons as Claim 1.

Claim 7 as amended recites "the third control signal causes different sets of delay trim units to be enabled during different cycles of the reference clock signal, thereby causing the generated clock signal to exhibit a repeating regular pattern of varying clock periods, wherein the pattern of clock periods includes the base clock period, as well as clock periods greater than and less than the base clock period."

As described above, Matsuzaki et al. teach a delay locked loop circuit, which delays a first clock, and generates a control clock having a predetermined phase relation with this first clock. (Matsuzaki et al., Col. 2, lines 30-33.) However, Matsuzaki et al. fail to teach that the control clock exhibits "a repeating regular pattern of varying clock periods" as recited by Claim 7. For this reason, Claim 7 is not anticipated by Matsuzaki et al.

Claim 8 recites "adjusting trim units in the delay line in a pre-determined pattern during consecutive clock cycles".

The Examiner argues that "The control signals (Q1~Q4) are predetermined patterns (see Fig. 18) being sent to the variable delay circuits (11, 13) to adjust the delay line (see, Fig. 15.)" However, Matsuzaki et al. teach that "counter 590 generates a delay control signal Q0-Q4 on the basis of either a count-up signal UP1 and count-down signal DOWN1 from the phase

comparator, or a delay set signal S0-S4 and delay reset signal R0-R4". (Matsuzaki et al., Col. 15, lines 28-32.) Thus, delay control signals Q0-Q4 can exhibit many different patterns during consecutive clock cycles, depending on the phase differences between the clock signals (c-clk and d-i-clk) applied to phase comparator 16. (See Matsuzaki et al., description of phase comparator 16.)

Because Matsuzaki et al. teach that the delay control signals Q0-Q4 can be adjusted in any number of different patterns in response to the clock phase differences, Matsuzaki et al. fail to teach "adjusting trim units in the delay line in a pre-determined pattern during consecutive clock cycles" as recited by Claim 8. For this reason, Claim 8 is not anticipated by Matsuzaki et al.

Claims 9, 17 and 18, which depend from Claim 8, are not anticipated by Matsuzaki et al. for at least the same reasons as Claim 8.

Claims Rejections Under 35 USC 103(a)

Claims 3 and 4 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong.

As described above, Claim 1 is allowable over Jeong. Claims 3 and 4, which depend from Claim 1, are therefore allowable over Jeong for at least the same reasons as Claim 1.

Claims 3 and 4 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki et al.

As described above, Claim 1 is allowable over Matsuzaki et al. Claims 3 and 4, which depend from Claim 1, are therefore allowable over Matsuzaki et al. for at least the same reasons as Claim 1.

Claim 6 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki et al. in view of Tomita (U.S. Patent No. 6,501,309).

As described above, Claim 1 is allowable over Matsuzaki et al. Claim 6 depends from Claim 1. Tomita fails to remedy the above-described deficiencies of Matsuzaki et al. Thus, Claim 6, which depends from Claim 1, is therefore allowable over Matsuzaki et al. in view of Tomita for at least the same reasons as Claim 1.

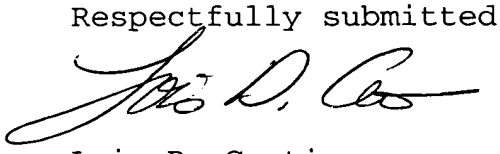
Objections to the Claims

Claims 11-16 have been objected to as being dependent on a rejected base claim. The Examiner has indicated that these claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants believe that base Claim 8 is allowable for the reasons recited above. For this reason, Applicants are not amending Claims 11-16 at this time.

CONCLUSION

Claims 1-4 and 6-21 are pending in the present application. Reconsideration and allowance of these claims is respectfully requested. If there are any questions, please telephone the undersigned at (720) 652-3733 to expedite prosecution of this case.

Respectfully submitted,



Lois D. Cartier
Agent for Applicants
Reg. No. 40,941

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Pat Slaback
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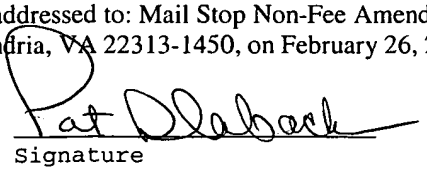

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